CLAIMS

What is claimed is:

1. A method for accessing configuration registers, comprising:

a) receiving an indication that an attempt has been made to access a first register, the first register to reflect an index variable that points to a configuration register; and then

b) receiving an indication that an attempt has been made to access a second register, the second register to reflect part of the contents of a configuration register to which the index variable points; and then

c) in response to b), and without waiting for another attempt to access the first register, changing the index variable to point to another configuration register.

2. The method of claim 1 wherein the attempt to access the first register is an attempt to write a given index value that points to a given configuration register,

and wherein the attempt to access the second register is an attempt to write a given content value that is to be part of the content of the given configuration register.

3. The method of claim 2 wherein one of the given index and content values as written to the first and second registers, respectively, is encoded.

4. The method of claim 3 wherein both of the given index and content values as written to the first and second registers, respectively, are encoded.

5. The method of claim 2 further comprising, after c):

d) receiving an indication of another attempt to access the second register; and then

e) in response to d), and before receiving yet another attempt to access the first register, changing the index variable to point to yet another configuration register; and then

repeating d)-e) to point to still another configuration register.

6. The method of claim 1 wherein in c), the index variable is changed only if a special mode of operation, for programming configuration registers via automatic indexing, has been entered.

7. A method for programming a plurality of configuration registers, comprising:

a) enabling a first mode of operation for an integrated circuit (IC) component in which a plurality of configuration registers are to be programmed according to b)-e);

b) writing to a first control register in said IC component to enable access to a selected one of the registers; and then

c) writing to a second control register in said IC component a content value for said selected one of the registers; and then

d) writing to the second control register a further content value for another selected one of the registers, without again writing to the first control register; and then

e) repeating d) until all of the registers have been programmed.

8. The method of claim 7 further comprising:

programming a further plurality of configuration registers by

f) disabling the first mode of operation; and then

g) writing to the first control register to enable access to a selected one of the further registers; and then

h) writing to the second control register a content value for said selected one of the further registers; and then

repeating g)-h) until all of the further registers have been programmed.

9. The method of claim 8 wherein the plurality of registers are programmed sequentially.

10. An integrated circuit (IC) component, comprising:

a plurality of configuration registers;

a counter to provide a first index value that can change by automatically incrementing or decrementing the counter;

multiplexor logic having a first input to receive the first index value, a second input to receive a second index value, an output coupled to index the

plurality of registers, the multiplexor logic to receive a control signal that indicates a mode of operation of the IC component, the mode being one in which the registers are to be indexed by automatically incrementing or decrementing the counter; and

detection logic having an input to receive a first hardware control signal that indicates a request has been received from outside of the IC component to access a configuration register, and an output to provide an increment or decrement signal to the counter.

11. The IC component of claim 10 wherein the first hardware control signal indicates that a request has been received to write a configuration data register of the IC component, and wherein the detection logic has a further input to receive a second hardware control signal that indicates a request has been received to read the configuration data register, the increment or decrement signal to be asserted in response to any one of the first and second hardware control signals being asserted.

12. The IC component of claim 10 wherein the counter has a further input to load itself with the first index value which has been obtained from a request, received from outside of the IC component, to write to a configuration address register of the IC component.

13. A computer system comprising:

a first processor and main memory combination;

a graphics subsystem; and

an I/O hub communicatively coupled to the first combination via a first point to point link, and communicatively coupled to the graphics subsystem via a second point to point link,

the I/O hub to act as a bridge between the first combination and the graphics subsystem component,

the I/O hub having a plurality of configuration registers the contents of some of which indicate how a transaction request received on one side of the bridge is transported to another side of the bridge, and wherein

the I/O hub further includes a counter to provide a first index value, multiplexor logic having a first input to receive the first index value, a second input to receive a second index value, an output coupled to index the plurality

of registers, the multiplexor logic to receive a control signal that indicates a mode of operation of the I/O hub, the mode being one in which the registers are to be indexed by automatically incrementing or decrementing the counter, and detection logic having an input to receive a first hardware control signal that indicates a request has been received from outside of the I/O hub to access a configuration register, and an output to provide an increment or decrement signal to the counter.

14. The system of claim 13 further comprising a second processor and main memory combination communicatively coupled to the I/O hub via a third point to point link, and to the first combination via a fourth point to point link, and wherein the I/O hub is to act as a further bridge between the second combination and the graphics subsystem.

15. The system of claim 14 further comprising a network interface controller communicatively coupled to the I/O hub via a fifth point-to-point link.

16. The system of claim 13 wherein the I/O hub further includes a configuration address register to contain a port number, function number, and register number that together point to a selected one of the registers, and a configuration data register to reflect part of the contents of the selected one of the registers.

17. A method for programming software-accessible registers, comprising:

a) detecting a first bus event, in a computer system, aimed at accessing an index variable that points to one of a plurality of software-accessible registers of the system, and a second bus event aimed at accessing the content of the register to which the index variable points; and then

b) changing to a block mode for programming some of the software-accessible registers; and then

c) detecting a third bus event, in the system, aimed at updating one of the registers to which the index variable points; and then

d) in response to c), and without waiting for another bus event aimed at accessing the index variable, changing the index variable to point to another one of the plurality of registers.

18. The method of claim 17 wherein the first bus event is to write a given index value to a first register of the system, the given index value points to a given one of the plurality of software-accessible registers,

and wherein the second bus event is to write a given content value to a second register of the system, the system to then write the given content value to the given software-accessible register.

19. The method of claim 18 wherein the given index and content values as written to the first and second registers, respectively, are encoded.

20. The method of claim 17 further comprising, after d):

e) detecting a fourth bus event to update said another one of the plurality of registers; and then

f) in response to e), and before receiving yet another bus event to update the index variable, changing the index variable to point to yet another one of the plurality of registers.

21. The method of claim 18 wherein first and second registers are mapped to a host CPU I/O address space of the system.

22. An article of manufacture comprising:

a machine-accessible medium having data that, when accessed by a machine, initiate a) a block mode of operation in which a first plurality of configuration registers are to be programmed in accordance with b)-d) below, and then b) a bus transaction to access a first control register, and then c) another bus transaction to access a second control register, and then d) a plurality of further bus transactions each to access the second control register without any further bus transactions to access the first control register.

23. The article of manufacture of claim 22 wherein the medium has further data that, when accessed by the machine, causes a return from said block mode to a normal mode in which a second configuration register is programmed by initiating a bus transaction to access the first control register and then another bus transaction to access the second control register.

24. The article of manufacture of claim 23 wherein the data treats the first and second control registers as being mapped to a host/CPU I/O address space.